# Access to Advanced Packaging and Test

**Brett Hamilton**

ELECTRONICS RESURGENCE INITIATIVE SUMMIT & MTO Symposium 2020 | Seattle, WA | August 18-20

## *Heterogeneous Integration & 2.5D/3D Packaging* — *Heterogeneous 3D*

## Background

**THE CHALLENGE**

**WE MUST INCREASE PERFORMANCE, WHILE ADDRESSING:**

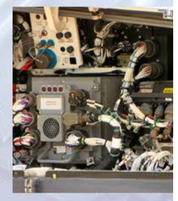
- Extremely high processing requirements
- Restrictions in size, weight & power (SWaP)
- Need to move terabytes of data in real-time
- Customize/optimized for DoD applications
- Reliability in DoD environments
- Must meet cost and schedule

**Heterogeneous Integration and Advanced Packaging Helps Addresses all These Challenges!**

https://www.navy.mil/navydata/aircraft/fa18/fa18aim9.jpg

US Navy makes history by landing unmanned drone on aircraft carrier

https://www.theguardian.com/world/video/2013/jul/11/drone-aircraft-carrier-video



Modernization under constrained SWaP

https://radschool.org.au/magazines/Avalon/Page2.htm




Source: Intel – Accelerating Innovation Through Chiplets OCP/ODSA Workshop, 6/10/2019

### World Leaders

**Industry Giants TSMC and Intel Vow to Focus on 3D IC Packaging** (1)

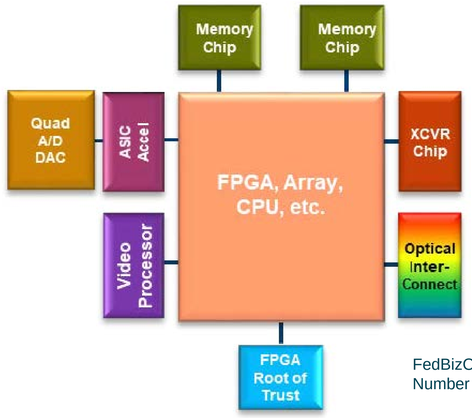
Demand for high-performance computing (HPC) chips is exploding. These super-speedy chips are critical for data centers and cloud computing infrastructures to support new performance-hungry technologies such as artificial intelligence (AI) and 5G……. Heterogeneous integration offers a potential answer as an advanced packaging technology designed to meet these skyrocketing performance demands on HPC chips and open the door to a whole new world of 3D integrated circuits (ICs).

(1) https://blog.semi.org/technology-trends/industry-giants-tsmc-and-intel-vow-to-focus-on-3d-ic-packaging

**So important are 3D ICs that Intel and TSMC representatives speaking at the recent Heterogeneous Integration Summit hosted by SEMI Taiwan in Taipei declared that the packaging technology will all but dictate the future of the industry.**

## Approach

### Leveraging SOTA: While Allowing Customization!




FedBizOpps.gov – Solicitation Number N00164119SNC10

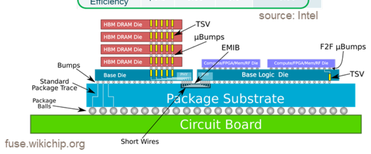
**Custom configurations of chiplets allows DoD to optimize SWaP and performance to meet specific DoD weapon system specification. This modular approach is critical for rapid technology transition and for intellectual property (IP) re-use, reducing cost.**

### SHIP Digital vs SHIP RF

**Digital – Focus on efficient, high density digital connectivity**

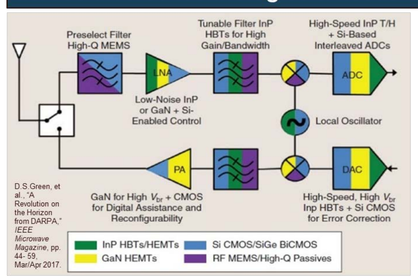
| Die - Die IO Interface Comparison | Units | AIB-Gen 1[1] (DARPA CHIPS) | MDIO Gen 1 | TSMC LIPINCON[3] |
|---|---|---|---|---|
| Technology (Technology Availability) | | EMIB (2017) | EMIB (2020) | CoWOS (2020) |
| Company | | Intel | Intel | TSMC |
| Pin Speed | Gbps | 2.0 | 5.4 | 8.0 |
| Minimum Bump Pitch | µm | 55 | 55 | 40 |
| Shoreline BW density | GBps/mm | 32 | 197 | 67 |
| PHY Power Efficiency | pJ/b | 0.85 | 0.5 | 0.56 |

source: Intel




fuse.wikichip.org

**RF – Focus on efficient RF performance across diverse technologies & needs**




D.S.Green, et al., "A Revolution on the Horizon from DARPA," *IEEE Microwave Magazine*, pp. 44- 59, Mar/Apr 2017.

**Technology *choices balancing*** RF performance **with maturity**

**Multiple semiconductors**

### *Solution*

**Technical Approach**

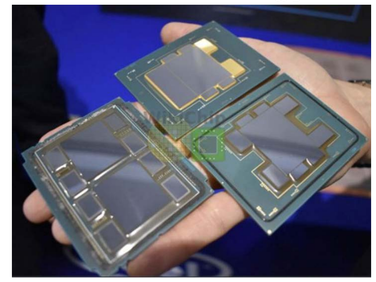
- Performance
- Capability
- Maturity
- Cost
- Scalability
- Market

**Infrastructure**

- Security
- Design Center
- Assembly & Test Center

## Results and Impact

### Technology is Commercially Available



https://www.tomshardware.com/news/intel-packaging-co-emib-odi-foveros-mdio,39840.html

**Intel** revealed three new packaging technologies at SEMICON West: These new technologies enable massive designs by stitching together multiple dies into one processor. Building upon Intel's 2.5D EMIB and 3D Foveros tech, the technologies aim to bring near-monolithic power and performance to heterogeneous packages.

https://fuse.wikichip.org/news/1833/a-look-at-necs-latest-vector-processor-the-sx-aurora/2/

NEC's Latest Vector Processor - The chip utilizes **TSMC**'s second-generation chip on wafer on substrate (CoWoS) technology with NEC's implementation developed in collaboration with TSMC and Broadcom.

**TRANSITION TO SHIP DIGITAL & RF**

**Develop domestic manufacturing capabilities for secure, SOTA, and reliable heterogeneous integrated packaging and test to meet the needs of the USG, including military and aerospace applications**

- **SHIP design center**
- **SHIP assembly and test center**

STRATEGIC & SPECTRUM MISSIONS ADVANCED RESILIENT TRUSTED SYSTEMS (S2MARTS) REQUEST FOR SOLUTIONS (RFS)

*in support of the*

STATE-OF-THE-ART HETEROGENEOUS INTEGRATED PACKAGING (SHIP) PROTOTYPE PROJECT

PROJECT NO. S2MARTS 19-06

*All prospective respondents must be members of the NSTXL consortium*

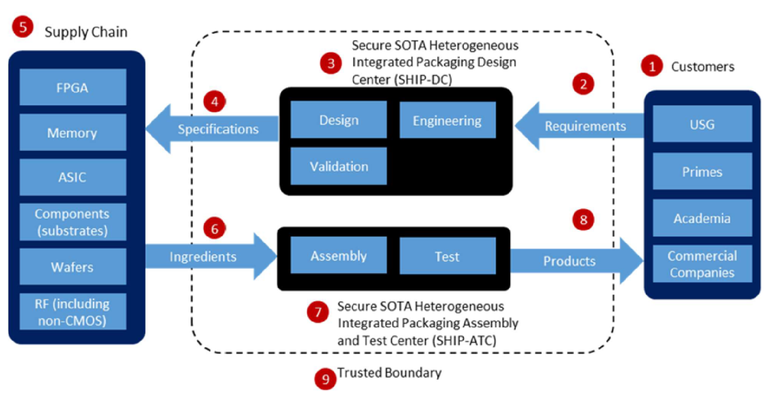
https://nstxl.org/opportunity/state-of-the-art-heterogeneous-integrated-packaging-ship-prototype-project/
https://s2marts.org/opportunities/#tab2a

Digital Phase 1:
- Xilinx
- Intel Federal

RF Phase 1:
- Keysight Technologies
- Qorvo Texas, LLC
- GE Research
- Northrop Grumman Systems

**Custom configurations that can include ASIC's and structured ASIC's allow the Primes to customize performance to meet their particular DoD weapon system specification. This is critical for rapid technology transition and sustainability.**

### SHIP Initiative




Notional design and prototype manufacturing flow for delivering secure and SOTA packaging meeting the needs of defense and aerospace applications.

FedBizOpps.gov – Solicitation Number N00164119SNC10